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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/531,860	03/21/2000	Jorge Humberto Figueredo	041-481-RB	6689

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EXAMINER
WEST, JEFFREY R

ART UNIT	PAPER NUMBER
2857	

DATE MAILED: 10/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Offic Action Summary	Application N .	Applicant(s)	
	09/531,860	FIGUEREDO, JORGE HUMBERTO	
	Examiner	Art Unit	
	Jeffrey R. West	2857	

-- Th MAILING DATE of this communication appears on the cover sheet with the correspondenc address --

P ri d f r Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *26 June 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3,5-8 and 10* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *10* is/are allowed.

6)☒ Claim(s) *1,3 and 5-8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *26 June 2003* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Drawings

1. The drawings are objected to as failing to comply with 37 CFR 1.84(p)(5) because they include the following reference sign(s) not mentioned in the description: "B1", "C", and "D". A proposed drawing correction, corrected drawings, or amendment to the specification to add the reference sign(s) in the description, are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

2. Applicant has not complied with the requirements for submitting omitted drawing pages. MPEP 601.01(d) reads as follows:

> If it is discovered that an application, located in a Technology Center (TC), was filed without all of the page(s) of the specification, and a Notice of Omitted Items has not been mailed by OIPE, the examiner should review the application to determine whether the application is entitled to a filing date. An application is entitled to a filing date if the application contains something that can be construed as a written description, at least one drawing figure (if necessary under 35 U.S.C. 113, first sentence), and at least one claim.
>
> Application Entitled to a Filing Date
>
> If the application is entitled to a filing date, the examiner should notify applicant of the omission in the next Office action and require applicant to do one of the following:
>
> (A) accept the application, as filed, without all of the page(s) of the specification;
>
> (B) file any omitted page(s) with an oath or declaration in compliance with 37 CFR 1.63 and 37 CFR 1.64 referring to the omitted page(s) and a petition under 37 CFR 1.182 with the petition fee set forth in 37 CFR 1.17(h), requesting the date of submission of the omitted page(s) as the application filing date; or

(C) file a petition under 37 CFR 1.53(e) with the petition fee set forth in 37 CFR 1.17(h) alleging that the page(s) indicated as omitted was in fact deposited with the USPTO with the application papers, including any and all evidence supporting the allegation. See MPEP § 503. The petition fee will be refunded if it is determined that the page(s) was in fact received by the USPTO with the application papers deposited on filing.

If applicant is willing to accept the application, as filed, without all of the page(s) of the application (item A above), an amendment of the specification is required to renumber the pages of the application consecutively and to cancel any incomplete sentences caused by the absence of the omitted page(s). The amendment should be submitted in response to the Office action.

Any petition filed in accordance with item B or C above should be filed with the TC. The TC will match the petition with the application file and forward the application file with the petition to the Office of Petitions, along with a brief explanation as to the page(s) of the specification that has been omitted on filing, for consideration of the petition in due course.

Applicant is requested to respond to this Office Action with appropriate corrections or documentation.

Claim Objections

3. Claims 1 and 3 are objected to because of the following informalities:

In claim 1, to avoid confusion, "in the internal components" should be —in the internal multi-chip components—.

In claim 3, the step marked "(e)" should be changed to —(d)—.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

4. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> **The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.**

5. Claims 7 and 8 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Claim 7 is considered to be vague and indefinite because it recites the confusing language, "range of room temperature to 20 degrees Celsius upward and 20 degrees Celsius downward to room temperature." In this limitation it is unclear whether the temperature starts and ends at room temperature or if the temperature starts at a value lower than room temperature, increases to room temperature, and returns back to the lower value. The first section of this limitation, "range of room temperature to 20 degrees Celsius upward" could possibly be interpreted as a range from room temperature to 20 degrees above room temperature. The second limitation, however, clearly describes starting at 20 degrees Celsius and ramping downward to end at room temperature. This is particularly confusing since room temperature is generally defined as a temperature approximately 20 degrees Celsius. For these reasons, claim 7 is rejected under 35 U.S.C. 112, second paragraph.

Claim 8 is rejected under 35 U.S.C. 112, second paragraph, because it incorporates the lack of clarity present in parent claim 7.

Claim R j ctions - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claims 1, 3, and 7, as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over ESPEC Technology Report, "Special issue: Evaluating Reliability and Measurement System" in view of U.S. Patent No. 5,107,325 to Nakayoshi and further in view of JP Patent No. 10-239373 to Agawa.

ESPEC teaches a method for testing a multi-chip IC package as a device under test, using temperature cycle testing in order to test for intermittent cracks, which lead to disconnection (i.e. open circuits) in its internal components (page 12, column 1, lines 18-39) comprising applying a rising temperature to the device under test while concurrently measuring the resistance during an up temperature ramp, at regular intervals, reducing down the temperature of the device under test back to starting room temperature while monitoring and reading the resistance, at regular intervals, plotting a graph of the resistance of the device during the temperature up ramp and during the temperature down ramp, and noting an erratic irregularity of the resistance plotted on a computer screen against temperature graphs in order to determine the intermittent defectiveness of components within the multi-chip

package clearly distinguishable from a normal set of components (i.e. sample a vs. sample b) (page 12, column 2, lines 31-47 and Figure 6). ESPEC also teaches determining the resistance using an ohmmeter (i.e. a device functionally equivalent and obviously exchangeable for a multi-meter), connected through an I/O socket (page 13, Figure 7). Further, since the invention shows that the resistance of the device under test returns to its original value when the temperature is returned to room temperature (Figure 6), the invention of ESPEC teaches non-destructive testing of the device for intermittent faults.

While the invention of ESPEC does teach performing temperature cycle testing by determining the occurrence of cracks based upon a resistance graph, ESPEC does not specifically disclose determining the occurrence of open and short circuits.

Nakayoshi teaches a packaged semiconductor device wherein the device is tested using temperature cycle tests that cause thermal stress due to a difference in the linear coefficient of expansion between semiconductor chips and the printed wiring board (column 3, lines 11-16). Nakayoshi also teaches performing the temperature cycle test in order to determine a plurality of deteriorations such as cracks, disconnection (i.e. open circuits), and short-circuits (column 7, lines 28-58).

It would have been obvious to one having ordinary skill in the art to modify the invention of ESPEC to include determining the occurrence of open and short circuits in addition to the occurrence of cracks, as taught by Nakayoshi, because ESPEC teaches evaluating the reliability of connections, as well as that the occurrence of cracks leads to the occurrence of open circuits, and the combination would have

provided more thorough analysis of the device connections thereby providing more intelligible diagnostic information to the user for aid in repair. Further, the invention of ESPEC discloses performing temperature cycle testing and Nakayoshi teaches that this type of testing also results in open and short circuit fault detection (column 7, lines 28-58).

While the invention of ESPEC and Nakayoshi teaches determining the occurrence of open and short circuits by measuring a change in resistance of a device, the combination does not specifically disclose the points on the device to measure the resistance.

Agawa teaches a short circuit checker used in packaging parts of printed circuit boards comprising attaching the printed circuit base to a test socket (0007) and monitoring the resistance between the power supply line (i.e. power bus) and common line (i.e. ground) in order to determine the occurrence of a short circuited, faulty component (0004) which is indicated by a non-linear, rapid change in resistance (0009).

It would have been obvious to one having ordinary skill in the art to modify the invention of ESPEC and Nakayoshi to include monitoring the change in power bus to ground resistance, as taught by Agawa, because Agawa suggests a method that would be applicable in the invention of ESPEC and Nakayoshi to determine when a change in temperature has caused a short circuit or similarly component failure in a quick, accurate, and non-destructive way (0011).

With respect to claim 7, while the invention of ESPEC, Nakayoshi, and Agawa doesn't specifically disclose data logging every two seconds, Applicant fails to provide the criticality for specifying that the measurements be logged every two seconds (page 18, lines 11-18) and therefore this feature is considered an engineering design choice. Further, the invention of ESPEC does disclose continuously measuring changes in resistance values in order to capture intermittent failures, as is the intent of the frequent logging in the instant invention. Further still, it is considered to be very well known in the art that the accuracy of resulting measurements is dependent on the number of data samples taken; therefore it would have been obvious to one having ordinary skill in the art to take measurements at any interval that produces the desired accuracy.

Similarly, with respect to the best interpretation of claim 7, Applicant intends to ramp the temperature to 20 degrees C above room temperature. Applicant fails to provide the criticality of increasing and decreasing the temperature 20 degrees and only describes adjusting the temperature within the non-destructive range of the device to determine non-linearity in resistance. As noted above, the invention of ESPEC keeps the device within its non-destructive range and determines this desired non-linearity. Further, while claim 7 requires a specific 20 degree change, the specification describes this as non-critical providing the ramping of 20 to 30 degrees to test any non-linearity of the resistance (page 11, lines 16-23 and page 14, lines 14-17). Similarly, Figures 3b, 4, and 5 describe embodiments of a change of more than 20 degrees Celsius. For these reasons, the specific interval and

temperature range, as best understood, are interpreted as non-critical aspects and the invention of ESPEC, Nakayoshi, and Agawa teach a functionally equivalent method.

8. Claims 5, 6, and 8 as best understood, are rejected under 35 U.S.C. 103(a) as being unpatentable over ESPEC in view of Nakayoshi and Agawa, and further in view of U.S. Patent No. 5,419,780 to Suski.

As noted above, ESPEC in combination with Nakayoshi and Agawa teaches many of the features of the claimed invention including controlling the temperature of a device under test but does not disclose controlling the temperature using a Peltier device.

Suski teaches a method and apparatus for recovering power from a semiconductor circuit using a well known Peltier-junction thermoelectric heat-reducing cooler which generates a temperature differential between two opposing surfaces (column 4, lines 59-62) wherein one of the surfaces is conductively connected, such as with a metallic shield or adhesive (i.e. temperature transfer block) (column 3, lines 61-64 and column 4, lines 5-8), to the surface of the device under test (column 5, lines 27-34). Suski also teaches connecting the Peltier device to a heat sink and corresponding fan (Figure 5),

It would have been obvious to one having ordinary skill in the art to modify the invention of ESPEC, Nakayoshi, and Agawa to include the specifics of a component to control the temperature of the device under test, as taught by Suski, because

Suski suggests a device necessary to accurately, and efficiently, carry out the cooling in the invention of ESPEC, Nakayoshi, and Agawa rapidly using a device common for semiconductor applications (column 2, lines 3-8 and column 4, lines 57-62).

Further, since the invention of ESPEC, Nakayoshi, and Agaya teaches setting the initial temperature of the device under test at room temperature and Suski teaches connecting the Peltier device to the device under test, the combination would have set the Peltier device and temperature transfer block at room temperature.

Allowable Subject Matter

9. Claim 10 is considered allowable over the cited prior art for the following reasons.

While the invention of ESPEC, Nakayoshi, and Agaya teaches many of the features of the claimed invention and further reference U.S. Patent No. 5,924,289 to Bishop, II, teaches controlled temperature cabinet system and method comprising a device for heating or cooling an ambient environment (abstract) based upon a programmable controller operating in conjunction with a temperature sensor (column 2, line 51 to column 3, line 1) that controls power to a fan and a Peltier-junction module acting as an increasing or decreasing heat source attached to a heat sink (column 2, lines 30-42 and Figure 3), none of the prior art teaches or suggests, in combination with the other claimed limitations for testing internal components of an integrated circuit package device, the specific connections between the measuring

components. More specifically, a control program for connection and management of a programmable controlled fan power supply, a programmable power supply, for controlling the addition of heat to or reduction of heat from the a temperature transfer block, and for sensing operations of a temperature meter and a digital multimeter.

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure:

U.S. Patent No. 5,924,289 to Bishop, II, teaches controlled temperature cabinet system and method.

U.S. Patent No. 6,196,002 to Newman et al. teaches a ball grid array package having a thermoelectric cooler as well as the idea that a change in 10-20 degrees Celsius may double the failure rate of integrated chip packages.

Love et al, High Density Packaging User Group International, "BGA Reliability Characterization Project Temperature Cycling Tests Final Report" teaches temperature cycling while monitoring changes in electrical resistance to test solder connections.

U.S. Patent No. 6,181,556 to Allman teaches a thermally-coupled heat dissipation apparatus for electronic devices.

U.S. Patent No. 5,290,710 to Haj-Ali-Ahmadi et al. teaches a method for testing integrated circuits on a carrier substrate.

U.S. Patent No. Re. 32,625 to Schwarz et al. teaches the dynamic testing of electrical conductors including plotting resistance vs. temperature.

11. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jeffrey R. West whose telephone number is (703)308-1309. The examiner can normally be reached on Monday through Friday, 8:00-4:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Marc S. Hoff can be reached on (703)308-1677. The fax phone

numbers for the organization where this application or proceeding is assigned are (703)308-7382 for regular communications and (703)308-7382 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703)308-0956.

jrw
September 17, 2003

MARC S. HOFF
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800